IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner: Le, D.
Wang et al.	Art Unit: 2818
Serial No. 10/053,256	
Filed: January 18, 2002	
For: TWO-STEP SOURCE SIDE IMPLANT FOR IMPROVING SOURCE RESISTANCE AND SHORT CHANNEL EFFECT IN DEEP SUB- 0.18um FLASH MEMORY TECHNOLOGY	

Commissioner of Patents
Washington, D.C. 20231

AMENDMENT AND REMARKS IN RESPONSE TO OFFICE ACTION

Sir:

In response to the Office Action mailed August 14, 2002, please consider the following remarks and enter the following amendments.

IN THE CLAIMS

Please amend the Claims as follows:

1. (Amended) A method of manufacturing a flash memory Electrically-Erasable Programmable Read Only Memory (EEPROM) device having a lightly-doped source region near the critical gate region and a heavily-doped source region away from the